112 Intro to Computer system 2019 Exam la o S Kmap TFIjf.jofD DoEDo oEnsTtB00 ol il lo B OO i oe f f f En Il o r l O lo o o L I Minterm En s B 1 En S A \_En s Bts A En CS B S A lb S so 1C

8 t

Diff

ii A a Et F

e aBi i

1

za A B CA'tB BGB

A B CA'tB B4B 1 D Al B't B Bl A Btc A BEA C D Ad Bl B B'so Al Al B CA CB c A B C

Al B CA A A

ATB De Morgan's Law 2b is s 420T Q r t Q Ii This is a one bit memory that scores

the value from input S Truth table when input SR is Ili S R Q Q1 S R Q Q Qnext Q'next 0 O l l l l 0 0 I I O l I 0 1 I O l O 1 I 0 O l l l l 0 I O l l U U l l l l o 0

iii Sychronous circuit is connected to a clock

signal and its output will only change based

on a change of clock Asychronous circuit doesn't have a clock and may have inconsistent output due to circuit gate delay Iv It's asynchronous V It with stone 1 in Q When CRS changes

from Cbo to 4,15 the result CQ Q's

will still stay the same as Ci o forever until LR S changes again vis The circuit will be in an unstable slate

and CQ Q's crook sway between CGD andco o

and CQ Q sway C dc o 2e is Seale Transition Diagram

J K Qe Qetl O O d O FK O l O 0 L o 0 I Qt O 00 O D ol O

o Il lo O

I I O l

O O th l O 1 I 0 I O l l

l l l 0 ii Minterme D Qter QE Te Qe K

1

F

t

Zd Spikes can occur when an asynchronous circuit

has a delay on input and the previous output has the same value as this delayed input When clock changes under this situation a spike with temporarily occur